

CLAIM AMENDMENTS

Please amend the claims by amending claims 40-41, without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment:

1.-31. (cancelled)

32. (previously presented) A non-volatile memory, comprising:
an array of memory storage units;
a plurality of sense amplifiers for sensing a group of memory storage units in parallel;
each of said plurality of sense amplifiers having properties dependent on operating environment and a set of control signals; and
a reference circuit having elements with properties representative of said plurality of sense amplifiers and sharing a common operating environment with said plurality of sense amplifiers, said reference circuit, responsive to said elements operating in the operating environment, generating said set of control signals such that said plurality of sense amplifiers are controlled to have its properties substantially insensitive to the operating environment.

33. (previously presented) The non-volatile memory of claim 32, wherein said properties include a threshold voltage of a component transistor.

34. (previously presented) The non-volatile memory of claim 32, wherein said properties include a capacitance of a component capacitor.

35. (previously presented) The non-volatile memory of claim 32, wherein said operating environment includes a given power supply.

36. (previously presented) The non-volatile memory of claim 32, wherein said operating environment includes a given temperature.

37. (previously presented) The non-volatile memory of claim 32, wherein said set of control signals includes a timing signal calibrated to a reference current.

38. (previously presented) The non-volatile memory of claim 32, wherein said set of control signals includes a voltage for controlling a voltage clamp.

39. (previously presented) A non-volatile memory, comprising:
a plurality of sense amplifiers for sensing a group of memory storage units in parallel, each of said plurality of sense amplifiers having properties dependent on operating environment and a set of control signals;

a reference circuit having elements with properties representative of a typical member of said plurality of sense amplifiers and located in a common operating environment with said plurality of sense amplifiers; and

means for generating said set of control signals, responsive to said elements operating in the operating environment such that said plurality of sense amplifiers is controlled to have its properties substantially insensitive to the operating environment.

40. (currently amended) The non-volatile memory as in any one of claims 32-39, wherein:

said plurality of memory storage units ~~[[is]]~~ are flash EEPROM.

41. (currently amended) The non-volatile memory as in any one of claims 32-39, wherein:

each memory storage unit stores one bit of data.

42. (previously presented) The non-volatile memory as in any one of claims 32-39, wherein:

each memory storage unit stores more than one bit of data.

43. (previously presented) A method of controlling a plurality of sensing circuits for a non-volatile memory, comprising:

providing a plurality of sense amplifiers for sensing a group of memory storage units in parallel, each of said plurality of sense amplifiers having properties dependent on operating environment and a set of control signals;

locating a reference circuit having elements with properties representative of a typical member of said plurality of sense amplifiers in a common operating environment with said plurality of sense amplifiers; and

generating said set of control signals, responsive to said elements operating in the operating environment such that said plurality of sense amplifiers is controlled to have its properties substantially insensitive to the operating environment.

44. (previously presented) The method as in claim 43, wherein:
said plurality of memory storage units is flash EEPROM.

45. (previously presented) The method as in claim 43, wherein:
each memory storage unit one bit of data.

46. (previously presented) The method as in claim 43, wherein:
each memory storage unit stores more than one bit of data.